Tunable Matching Circuit

Stanley S. Toncich

Related Applications

This application claims the benefit of U.S.
Provisional Application 60/283,093, filed April 11, 2001,
which is hereby incorporated by reference. In addition,
this application relates to U.S. applications "Tunable
Ferro-electric Filter," filed on July 13, 2001, "Tunable
Ferro-electric Multiplexer," filed on July 24, 2001, and
"Low Loss Tunable Ferro-electric Device and Method of
Characterization," filed on August 8, 2001, which are
hereby incorporated by reference.

BACKGROUND

Description of Related Art

Matching circuits are widely used to transform the
impedance of the various components within a circuit to a
target impedance. The input to the matching circuit may be
an RF signal, carrying information. The output to the
matching circuit may also be an RF signal, carrying
information. The matching circuit may precede or follow a
component. The component has an input and an output

impedance. If the component follows the matching circuit in the signal path, the target impedance of the component is its input impedance. If the component precedes the matching circuit in the signal path, the target impedance of the

5 component is its output impedance.

The matching circuit functions to set the impedance seen by the signal to the target impedance by compensating for the difference between the impedance of interest and the target impedance. The compensation of the impedance is

10 determined by the capacitance and the inductance of the matching circuit and by the configuration of the matching circuit. A wide range of impedance matching and transfer function circuits can be realized by using lumped element inductors or capacitors or both. At higher frequency (above

15 about 1 GHz) it is often advantageous to replace either lumped element inductors or capacitors or both with distributed transmission line networks. The usefulness of this replacement is also dependant on the dielectric constant (DK) of the substrate, as well as area

20 constraints.

Different arrangements of matching circuits are well known in the art. Some examples are: series capacitor, shunt capacitor; series capacitor, shunt inductor; series inductor, shunt capacitor; etc. A common configuration for

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a matching circuit is shunt capacitor, series inductor, shunt capacitor. Tranformers, and even resistive networks, can be used, if the insertion loss can be tolerated.

5 In general, matching circuits should have minimum added loss to prevent added degradation in the information signal. Excess loss increases the demands made on other components in an electronic system, especially the active elements such as amplifiers. In some cases, like at the input to a low noise amplifier (LNA), increased signal loss

10 cannot be made up (compensated for) by simply increasing the gain of the LNA.

The impedances of the components and the matching circuits are frequency dependent. The impedance is only matched at a single operating frequency, or over a limited

15 band of frequencies. If the designer wishes to operate the device at more than one frequency band, compromises must be made.

Antenna matching networks in wireless handsets will serve as an example. Since present dual band handsets

20 typically use only a single antenna, the present solution is to match impedances at a frequency in the middle of the range of operating frequencies. The impedance is mismatched at all frequencies besides the middle frequency. This increases power loss in either band.

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A second option is to use different components and
matching circuits for different operating frequencies. The
impedance match may be better this way, but the extra cost
of manufacturing and overall size of the combined circuit

5   may be prohibitive. It will be appreciated that if one of
each component could be well matched at all desired
operating frequencies, there would be a great savings in
circuit size and power consumption. A tunable matching
circuit would solve this problem.

10   In code division multiple access (CDMA) handsets,
matching circuits are required between the duplexer and
antenna (single band phone) or the diplexer or multiplexer
and antenna in dual or multi-band handsets as well as
before and after power amplifiers (PA's) and low noise

15   amplifiers (LNA's).

Prior to the invention, low loss tunable matching
circuits at frequencies above about 200 MHz had not been
achieved, although attempts had been made. Those attempts
include matching circuits using varactor diodes as shown in

20   U.S. pat. No. 6,198,441 B1, hereby incorporated by
reference. Specifically, a circuit comprising a series
inductor and a shunt varactor diode has been used to make
tunable matching circuits. The problem with this circuit
though, is that the losses are intolerably high,

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particularly for use in a portable communication device. Further, varactor diodes are quite temperature sensitve, and have proven to possess uncertain rf performance from lot to lot. It will be appreciated that a low loss tunable

5   matching circuit would be useful in many applications, but particularly in a portable wireless communication device.

10   **SUMMARY**

The objective of this invention is to provide a low loss tunable matching circuit. The matching circuit may be for use in portable wireless communication devices. Low-

15   loss tunable f-e components may be used to make a matching circuit. This may be accomplished by using a f-e tunable capacitor or inductor. Matching circuits can be implemented by lumped elements placed in series or shunt or by distributed network elements or by some combination of the

20   two. In distributed element matching, f-e films can be used in planar (microstrip, stripline, CPW, among others) passive matching circuits to vary the permittivity of the underlying substrate, thus effecting a change in the matching circuit's or resonator's electrical length. The

25   use of planar matching circuits is familiar to anyone trained in the art of amplifier or circuit design. The matching networks here can be hybrids and couplers as well

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as the more conventional distributed inductive and capacitive structures.

The advantages of the invention include lower insertion loss of the matching circuit and a better impedance match resulting in lower insertion loss of the component or components being matched. Furthermore, better matching means that there will be less interference due to reflection within a circuit.

Additionally, portable wireless communication devices will have longer battery lifetimes and talk times.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a is a plan view of a ferro-electric gap capacitor.

FIG. 1b is a cross-sectional view of the ferro-electric gap capacitor of FIG. 1a taken along line A.

FIG. 2a is a plan view of a ferro-electric overlay capacitor, along with an accompanying DC blocking capacitor.

FIG. 2b is a plan view of the first metal layer in the overlay capacitor of FIG. 2a.

FIG. 2c is a cross-sectional view of the overlay capacitor of FIG. 2a taken along line B in Fig. 2a.

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Figure 3 illustrates an enlarged view of a portion of Figure 2a.

Figure 4a is a plan view of a ferro-electric interdigital capacitor.

5   Figure 4b is a plan view of a ferro-electric microstrip inductor.

Figure 4c is a schematic diagram equivalent circuit to the inductor shown in Figure 4b.

Figure 5 is a schematic of an exemplary matching
10   circuit.

Figure 6 is a schematic of an exemplary matching circuit.

Figure 7 is a schematic of an exemplary matching circuit.

15   Figure 8 is a schematic of an exemplary matching circuit.

Figure 9 is a schematic of an exemplary matching circuit.

Figure 10 is a schematic of an exemplary matching
20   circuit.

Figure 11 is a block diagram of a low loss tunable ferro-electric matching circuit.

Figure 12 is a block diagram of a matching circuit and surrounding circuitry for an amplifier.

5   Figure 13 is a block diagram of a matching circuit between an antenna and a duplexer.

Figure 14 is a block diagram of a matching circuit between an antenna and a diplexer.

Figure 15 is a block diagram of a control source and a
10   matching circuit.

Use of the same reference symbols in different figures indicates similar or identical items.

DETAILED DESCRIPTION

15   The objective of this invention is to provide a low loss tunable matching circuit. Low-loss tunable f-e components may be used to make a matching circuit. This may be accomplished by using a f-e tunable capacitor or, to a limited extent, an inductor. Matching circuits can be
20   preferably implemented by lumped elements placed in series or shunt or by distributed network elements or by some

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combination of the two. In distributed element matching,
thin or thick f-e films can be used in planar (microstrip,
stripline, CPW, among others) passive matching circuits to
vary the permittivity of the underlying substrate, thus
5   effecting a change in the matching circuit's or resonator's
electrical length or characteristic impedance. The use of
planar matching circuits is familiar to anyone trained in
the art of amplifier or circuit design. The matching
networks here can be hybrids and couplers as well as the
10   more conventional distributed inductive and capacitive
structures.

      If lumped element matching components are used, then
f-e based tunable capacitors can be used in a similar
manner to effect a change in an amplifier's matching
15   network. Matching circuits are well known to those in the
art. A preferred matching network with lumped elements
would be the same as those known in the art, except that a
f-e material would be used to change the capacitance of a
capacitor.

20   The design of f-e tunable capacitors for use in
matching circuits will now be described. The total loss of
a capacitor, L_t, whether tunable or not, is given by a ratio
of its dissipated to stored energy, where the energy is
stored in the electric field and dissipated in resistance,

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i.e., L_t = (dissipated energy)/(stored energy). The inverse
of this loss is the quality factor, Q_c. For a capacitor, L_t
can be given by the quantity $(\omega * R_s * C)$, where ω is the
frequency in radians, R_s is the series resistance of the

5 capacitor, and C is the capacitance. For example, for a
1.0pF tunable capacitor to have a Q_u = 250 at 2.0 GHz
requires that R_s be .32 Ω (ohms). To minimize loss (obtain
a low R_s), requires an accounting of all loss mechanisms
present and an elimination of these loss mechanisms if

10 possible.

The loss determination of a f-e capacitor does not
depend on its topology, i.e, whether it is an overlay, gap,
or interdigital (IDC) capacitor.

15 For f-e devices, the total loss is governed by summing
each source contribution as follows:

$L_t = L_{geom} + L_{attach} + L_{metal} + L_{sub} + L_{rad} + L_{meas} + L_{f-e};$

where L_{geom} is derived from the topology of the
capacitor,

20 L_{attach} is loss due to device attachment,

L_{metal} is the total metal loss,

L_{sub} is the base substrate loss (if present),

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L_{rad} is the radiation loss, both desired and undesired,

L_{meas} is the total loss arising from measurement errors, and

L_{f-e} is the f-e loss tangent.

5   This loss allocation can first be used to obtain an accurate value of L_{f-e} (or f-e tan δ) at the desired operating frequency in the manner in which the f-e capacitor will be used. To correctly derive L_{f-e}, one must eliminate or constrain all of the other loss contribution

10   sources just described. For example, L_{geom} will vary according to topology, being best for an overlay capacitor, worse for a gap capacitor, and much worse for an IDC capacitor. Although this loss can be reduced and controlled, it is inherent to a device. Consequently, the

15   choice of topology for a given f-e capacitor will affect the best possible Q_c attainable from the f-e capacitor. Electromagnetic (EM) software can establish a baseline loss for a desired geometry, assuming a lossless f-e film. This baseline loss represents the best (lowest) loss for a given

20   geometry.

In general, a gap capacitor is easiest to fabricate. An IDC is next easiest, and an overlay capacitor is hardest

of these three. Compared to an IDC, the gap capacitor will have a better Q but lower capacitance per unit cross section (W in Fig. 1a). The IDC's capacitance is greater due to the use of a number of fingers per unit cross

5   section. For many communication filter applications, however, large capacitance (C ≥ 4.0 pF) is not needed. Thus, a gap capacitor often can provide adequate capacitance. The inherently high value of κ for most f-e films helps provide relatively high capacitance per unit cross section, W,

10   compared to a conventional gap capacitor.

L_{attach} arises from discrete device attachment techniques, including, for example, solder, silver paint, or wire bonding. These attachment losses may be large and unpredictable. The lowest losses are achieved by direct

15   fabrication of the f-e capacitor to the resonator or other RF circuitry, thus minimizing if not eliminating this loss component.

The inherent loss of a stand-alone f-e capacitor is of little consequence. What is of much greater consequence is

20   any added loss arising from the attachment of the f-e capacitor to a circuit. Even if the f-e capacitor were lossless, should a large loss connection be used, the overall effect is that of a lossy f-e device. For example,

if a $Q \geq 250$ at 2.0 GHz is desired for a capacitance of 1.0

pF, then the total series resistance R_s must be ≤ 0.32 ohm.

Any additional loss will thus further reduce the Q of this

capacitor. That this additional loss is external to the

5   actual capacitor is irrelevant. Even unavoidable loss

mechanisms, such as those due to mounting, for example,

lower the effective Q of the capacitor from the perspective

of its effect on the system.

For minimum added loss, the connection between the f-e

10   capacitor and the resonator should provide the lowest added

resistance. Thus, the electric currents and charges

associated with the f-e capacitor should see a minimum

added loss. Conventional bonding or mounting techniques,

such as (but not limited to) soldering, wire bonding or

15   silver paint or paste do not provide for such a low loss,

controllable bond.

The added, unpredictable loss arising from the use of

such bonding methods degrades the realized Q regardless of

whether or not the f-e capacitor is being used for

20   resonator tuning purposes or characterization of an f-e

film.   Thus, for best performance (lowest loss) the f-e

capacitor structure should be directly fabricated onto or

with the resonator it is meant to tune or onto other

essential RF circuitry. Only by direct fabrication can

there be a minimum loss transition for electromagnetic (EM)

sources (currents) from the f-e tuning elements to the

resonator. The desirable effects of direct f-e capacitor

5   fabrication onto or with a resonator can be enhanced by the

lack of sharp corners or transitions.

Factors for L_{metal} include the surface roughness (SR) of

the metal, metal thickness as compared to skin depth, δs,

and conductivity. SR may be effectively eliminated as a

10   factor if SR is less than aproximately 10 micro inches root

mean square (rms) for operating frequencies in the L and S

band (1-4 GHz). The metal thickness may be reduced as a

factor if the thickness is $1.5\delta s$ or greater, or effectively

eliminated if the thickness is $\geq 5\delta s$. For electrode

15   contacts, metal thickness (t_m) can be approximately $1.5\delta s$.

For the case of electromagnetic resonators, where a

travelling or standing wave must be supported, i.e., where

the metal in question extends for an appreciable fraction

of a wavelength (about 10% or greater), the metal thickness

20   should be closer to about $5\delta s$ or greater.

Conductivity is best for silver, copper and gold (Ag,

Cu, and Au, respectively). Thus, L_{metal} can be reduced and

controlled, but not eliminated as a factor. Its effect,
however, can be calculated by expressions well known to
those skilled in the art, or by using line calculator tools
available in commonly used circuit simulators, such as
5 Eagleware or Touchstone. Further, precise fabrication
control can bound geometric variations in L_{metal}.

The loss contribution represented by L_{sub} may be
minimized by choosing a low loss substrate with a loss
tangent less than 0.001 and preferably less than 0.0005 at
10 the operating frequency of interest. Suitable materials
include >99% pure alumina, a best current choice for
loss/cost benefits. Sapphire or MgO are better than
alumina in that they have lower loss tangents, but they are
more expensive. All these materials will accept f-e thin
15 films without buffer layers and have a surface roughness
that is acceptable with little or no further polishing.
Semiconductor substrates are poor choices because of their
relatively high conductivity. In addition to the factors
of loss tangent, surface roughness and price, suitable
20 substrates should not be brittle, can be fabricated as
larger area wafers, and can be easily metallized without
extensive pre-processing.

Separating out L_{sub} from the total loss of a composite

substrate (f-e film plus substrate) can be achieved by

using EM field or circuit simulation software. For

example, Sonnet, Momentum, or IE3D may be used. Thus, L_{sub}

5   can be reduced significantly and calculated precisely.

L_{rad} can be eliminated by proper shielding and design,

and so is typically not a factor. It should be noted that

a wide variety of filters, especially planar filters such

as combline or hairpin, depend upon radiative coupling to

10   achieve their desired performance. In these cases, one

should ensure that the unwanted, stray coupling is reduced,

if not eliminated.

L_{meas} can add significantly to the circuit loss

error because small, added loss significantly reduces the

15   measured Q of the device-under-test (DUT) or system thus

obscuring the intrinsic Q of the DUT. The conventional

method for measuring dielectric constant and loss tangent

in a material is the cavity perturbation technique, which

is well known to anyone skilled in the art. At L-band,

20   however, the size of the cavity becomes quite large. When

characterizing thin films (as opposed to bulk) with film

thickness ≤ 1.5 μm, such as f-e films, the problem becomes

very difficult as measurement errors can be severe.

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Furthermore, one should characterize an f-e capacitor (or filter) in a manner most similar to how it will be used. Thus, the preferred way to characterize f-e compounds or films is by microstrip resonator techniques.

5   For the purposes of determining f-e film characteristics and characterizing f-e capaictors, microstrip techniques are preferred to, for example, stripline or other volumetric techniques for f-e film characterization for the following reasons:

10   1)   Microstrip circuits are planar systems with no top cover, so no bonding of hard substrates as top covers is required. So there is also no need for continuity of ground planes (top to bottom) as needed in a stripline, for example.

15   2)   Preferably gap capacitors, and alternatively, IDC's, can be readily fabricated and measured.

       3)   A large body of knowledge exists as to the characterization of microstrip resonators.

       4)   No complex fixturing or fabrication or both are
20   needed as are required for dielectric cavities, for example.

One should measure high-Q circuits using resonator
techniques because broadband measurement may not accurately
resolve sub-ohm resistive losses at RF/microwave
frequencies with any accuracy. For the same reason, LRC
5   meters are not a good choice.

Measurement at radio frequency is requried to
correctly obtain Rs and consequently Q, for an f-e
capacitor, since low frequency measurement, especially
those below about 10 to 100 MHz, is dominated by a large
10   parallel resistance, Rp, that shunts the capacitance in
question. The dominance of Rp, along with the relatively
small values of the capacitance in question ($\leq$ 4.0 to 5.0
pF) prevents reliable Q (and therefore Rs) measurement at
low frequencies.

15   When used to measure losses, wafer probe stations must
be carefully used because it is difficult to calibrate out
resistive and inductive loss at RF/microwave frequencies.
Probe tips along with their ground connections are also
sensitive to placement on the DUT as well as the pressure
20   used to apply them. As a consequence, it is better to use
a resonant test circuit that allows for direct measurement
of the desired parameters in a way that does not require
individual device loss measurements.

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Thus, for measurements on resonant circuits, a network analyzer is the preferred choice. To minimize measurement loss and attain the most accurate measurement, one should calibrate out loss to the DUT, perform a full two port
5 calibration of the network analyzer, and use averaging for calibration and measurement. Finally, proper analysis of the measured data, such as that outlined in "Data Reduction Method for Q Measurements of Strip-Line Resonators," IEEE Transactions in MTT, S. Toncich and R.E. Collin, Vol. 40,
10 No. 9, Sept. 1992, pp. 1833-1836, hereby incorporated by reference, is required to accurately extract the Q, or loss, of the capacitor under test.

Using the results of above discussion to minimize, eliminate, or bound each of the foregoing losses, the total
15 loss may be re-expressed as:

$$L_t = L_{geom} + L_{metal} + L_{f-e} + \Delta L_{misc}$$

As discussed above, both L_{geom} and L_{metal} may be quantified and removed analytically to obtain an accurate measure of L_{f-e}. L_{geom} can be determined from an accurate electromagnetic simulation of the circuit based on a
20 lossless f-e material assumption. L_{metal} can be determined using the expressions for metal loss assuming conductivity,

SR (if applicable), and skin depth. The final term, ΔL_{misc}, represents a combination of the incomplete removal of the other loss mechanisms or from the finite bounds on or incomplete removal of L_{metal} and L_{geom} or both. As such it represents an irreducible error term. For accurate measurements of f-e film/component properties, it should be minimized and bounded, as described in the preceding sections.

Finally, to reduce the effect of L_{f-e} to a minimum one must use selective f-e film deposition to place the f-e film only in regions where it is needed for tuning and nowhere else.

The process of accounting for all loss mechanisms and eliminating or bounding these losses not only determines f-e loss but also establishes correct design guidelines for low-loss tunable filters. Knowledge of L_{f-e} gives the designer a baseline for the f-e film that is necessary for doing any type of optimum design using f-e films. This knowledge is necessary if one is to effectively trade-off loss tangent for tunability, for example. In short, accurate fabrication and measurement techniques result in consistent f-e film loss characterization and application.

Given the above techniques for minimizing loss,

preferred embodiments for the three types of f-e capacitors

may now be discussed. It will be appreciated, that

although these designs are for use in the L band (1-2 GHz),

5   the teachings of the present invention may be used to

design f-e capacitors for other frequency bands.

A preferred f-e tunable gap capacitor 10 is shown in

Figure 1a and 1b for use in the cellular band (800 to 1000

MHz) and the L-band (1-2 GHz) for wireless handsets. The

10   gap capacitor 10 is preferably formed on a ≥ 99% pure, 0.5

to 1.0 mm thick alumina, MgO, or sapphire substrate 12,

having an SR less than a 5.0 micro inch RMS. Alternatively,

the gap capacitor can be directly patterned on the front or

rear face or a side-wall of any number of resonators

15   structures. Examples are coaxial, monoblock or stripline

resonators. Such a capacitor should be fabricated as close

to its point of electrical connection to the resonator as

possible.

The substrate 12 may have a metal ground plane 14

20   depending on other requirements. However, the preferred

embodiment is without a ground plane to minimize stray

capacitance. Preferably, a f-e layer 16 of approximately

0.1 to 2.0 microns in thickness formed of BSTO or other

suitable or desirable f-e material for maximum capacitance

and tuning range is deposited on the substrate 12. More

preferably, layer 16 is 0.5 to 1.0 microns in thickness.

The Ba/Sr fraction, doping, alloying, mixing with other

5   components, and/or annealing determine the desired tuning

characteristics and loss (tan δ), and therefore Q also.

Generally, it is preferred that the tuning

characteristics meet the minimum required tuning range with

the minimum tuning voltage. Preferably, $x = 0.5$ in the

10   $Ba_xSr_{1-x}TiO_3$ composition for room temperature operation,

regardless of doping with other elements and pre- or post-

process annealing. It will be appreciated that other f-e

materials beside BSTO may be used as well. A metal layer

18 formed on the f-e layer 16 defines a gap 20 that is

15   preferentially 3.0 to 5.0 microns wide. Preferably, metal

layer 18 is 0.5 to 6.0 microns thick. More preferably,

metal layer 18 is 1.5 to 2.5 microns thick. It will be

appreciated that the gap 20 can be wider or narrower than

this range depending on requirements and processing

20   equipment. For minimum added loss in the PCS band, the

resulting capacitance will be approximately 0.6 pF to 1.5

pF at 0 volts DC while for the cellular CDMA band it will

be about 1.0 pF to 3.0 pF. The width of the capacitor, W

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17, will further determine the f-e capacitance, depending

on the particular f-e film used and the desired gap 20.

The width will typically be from .25 mm to 2.0 mm. The

capacitance is typically 0.6 to 3.0 pF. The resulting

5 capacitor should provide a Q of at least 160 at 2.0 GHz.

To minimize the added loss from the f-e film,

selective deposition or etching or both must be used, i.e.,

the f-e film is located only where needed for tuning and

nowhere else as stated above. For example, in the gap

10 capacitor 20 of Figure 1a, one could deposit the desired f-

e film 16 in a narrow region D_{f-e} around the gap 20, as

shown in Fig. 1a. D_{f-e} should be large enough to ensure that

the gap 20 can be repeatedly patterned over the f-e film in

manufacturing (allowing for mask alignment tolerance) and

15 to cover the needed area under the gap 20 for tuning

purposes. For the L-band PCS filters, $D_{f-e} = 0.2$ to 0.5 mm is

adequate with 0.2 mm preferred. As the operating frequency

increases D_{f-e} can decrease. As the operating frequency

decreases, D_{f-e} can increase.

20 F-E film properties and fabrication will play a

significant role in overall capacitor loss. Many techniques

exist to mitigate and minimize f-e film loss. One feature

of f-e films is that f-e film loss and tunability usually

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have an inverse relationship. That is, they usually must be

traded off against each other. The greater the f-e κ tuning

range, the greater the f-e loss in most cases.

Thus, even though f-e materials can achieve a κ tuning

5   range of about 3 to 1, less tuning may be acceptable for a

given matching circuit application. In that case, less

tuning would be chosen, with the benefit of less loss.

The effect of κ tunability on frequency tunability is

determined by the matching circuit topology. This effect

10 must also be considered in choosing an f-e material. But

without accurate characterization of the f-e loss to f-e κ

tunability trade-off, it will be difficult for a designer

to choose an optimum f-e material. Accurate

characterization of this trade-off allows a designer to

15 choose an optimum f-e material (providing the lowest loss

while meeting the tuning requirements).

With respect to L_{geom} for a gap capacitor, the major

contributions to loss are the four corners formed by the

gap.   These losses can be reduced by rounding the corners.

20   In comparison to gap and interdigital capacitors, an

overlay capacitor has the lowest L_{geom}. An overlay capacitor

is an example of a parallel plate geometry where the plate

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dimensions (length and width) are much greater than the plate separation. Given such a geometry, most of the electric field between the plates is uniform except for fringing along the edges. The fringing effect can be

5   reduced significantly by the use of a guard band, as is well known in the art. Thus, the geometric loss from a parallel plate capacitor is quite low. In addition, parallel plate geometries can provide high capacitances along with high tuning from small control voltage swings.

10   A preferred overlay capacitor 30 is illustrated in Figures 2a, 2b, 2c, and 3 that minimizes contributions to L_{geom}. The capacitor 30 is deposited directly on a 25 mil alumina substrate 31. A first metal layer 34 bonds to the substrate 31. The shape of metal layer 34 is also

15   illustrated in Figure 2b. A ferro-electric layer 36 overlies the metal layer 34. To form the overlay capacitor 30, a metal pad 40 formed on the ferro-electric layer 36 overlaps a portion of the first metal layer 34. Figure 3 illustrates an enlarged view of the overlapping portions.

20   Both the metal pad 40 and the metal layer 34 have a tapering region that forms an overlay capacitor 30 of the appropriate capacitance. An additional metal pad 41 overlaps the metal layer 34 to form a DC blocking capacitor

42. The metal pad 41 is tapered to form an appropriate capacitance for the DC blocking capacitor 42.

Due to the high dielectric constant (κ) of the most likely f-e films to be used, the overlay capacitor 30 may be quite small in area and still provide a capacitance (C_{f-e}) of 1.5pF. A bonding bias pad 44 is provided for attachment of a high value (500-1000kΩ) chip resistor. Note that the f-e film is deposited not only under the overlay capacitor 30 but also the blocking capacitor 42. However, the effect on the capacitance (C_{DC}) of the DC blocking capacitor 42 is irrelevant if $C_{DC} \geq 180$ pF and $C_{f-e} \leq 1.5$ pF, even under maximum V_{DC} bias (preferably 10V DC). This is because the DC blocking capacitor has a high enough capacitance that even when the capacitance is reduced by f-e tuning, it still has a minimal effect on C_{f-e}.

In such an embodiment, $0.7 \leq C_{f-e} \leq 1.5$ pF, f-e κ is approximately 1000, the overlapped portion of the metal pad 40 forming the overlap capacitor 30 is approximately 7.0 μm X 7.0 μm, and the f-e film thickness is approximately 1.0 μm. The metal layer 34 may be Pt and have a thickness of ≤ 0.5 μm. The metal pads 40 and 41 may be Ag and have a thickness of approximately 1.5-2.5 μm.

While thin film (t_{f-e} less than about 1.5 μm) f-e materials have been discussed, thick film f-e material can be used as well. Here, "thick film" is defined to be t_{f-e} greater than about 1.5 μm and less than about 1.0 mm. Bulk

5   is greater than about 1.0 mm. The fabrication and application of thick film f-e material is quite different than that of thin film f-e material. It usually involves a paste or a sol-gel technique, and the f-e materials to produce the significantly added thickness. The added

10   thickness and especially reduced cost comes at the price of somewhat degraded f-e performance, notably, reduced tunability.

While the L_{geom} of an overlay capacitor is lower than that of a gap capacitor, L_{f-e} of an overlay capacitor may be

15   higher, as all of the rf field is concentrated in the f-e film. In a gap capacitor the rf field is partially in air, partially in the f-e film and partially in the substrate. For the same reasons, an overlay capacitor has greater capacitance tunability for a given applied voltage than a

20   gap capacitor.

For a given cross sectional area, an IDC can provide a higher capacitance than a gap capacitor. It is more lossy, however, with the main contributions to L_{geom} including the

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gap spacing; loss increases as the gap spacing decreases.

Similarly, loss increases as finger width decreases.   The

finger length also affects loss with loss increasing as

finger length increases; especially in a microstrip (the

5   most common) realization of an IDC as the odd mode loss

dominates in such a structure.   In addition, loss increases

as the number of fingers increases due to loss introduced

from the additional sharp corners; note that increasing the

number of fingers is typically used to increase the

10   capacitance of an IDC.

Many investigators in the f-e area have used IDC's

with narrow finger widths and gaps (≤ 5.0 μm for each) to

characterize f-e film. This is problematic, as such an IDC

structure gives a high L_{geom} and therefore a low Q by itself.

15   Typically, Q is much less than 100 at 2.0 GHz for about 1.0

pF, even without any L_{f-e}. This makes it quite difficult to

measure L_{f-e}. The wide spread use of broad band measurement

techniques, as described above, further obfuscates any L_{f-e}

measurement.

20   A preferred IDC capacitor 60 is illustrated in Figure

4 that minimizes the contributions to L_{geom}. It is formed on

a 99.5 % pure alumina, MgO, sapphire or other suitable

substrate 62 of thickness of approximately 0.2 to 1.5 mm.

28

A f-e layer 64 is formed on the substrate 62. An input

port 66 and output port 68 couple to the IDC capacitor 60.

A metal layer 70 having a thickness of 1.5 to 3.0 microns

and deposited on the f-e layer 64 forms a gap spacing 72 of

5   approximately 5.0 microns and a finger width 70 of about

150 microns, or greater if possible.

A tunable inductor that can be used to create a

tunable matching circuit will now be described. Microstrip

inductors can be fabricated as short lengths, l, of narrow

10   lines as shown in Fig. 4b. Fig. 4b shows a microstrip

inductor 700 electrically connected to and situated between

two portions 702 and 704 of microstrip line. The width, W_L,

and length, l_L, are shown in Fig. 4b. Input and output

planes A and A' are also shown, for reference to a circuit

15   model shown in Fig. 4c and to be described later.

Note that,

$$l_L = \frac{\lambda_g}{4}, \text{ where}$$

$$\lambda_g = \frac{\lambda_o}{\sqrt{\varepsilon_{eff}}};$$

ε_{eff} = the effective dielectric constant;

20   $$\lambda_o = \frac{c}{f}; \text{ and}$$

c = the speed of light.

29

The inductor 700 has an inductance, L, given by the following equation:

$$L = \frac{Z_o}{\varpi} \sin\left(\frac{2\pi l}{\lambda_g}\right), \text{ where}$$

Z_o = the characteristic impedance of the narrow,

5   inductive line; and

$\varpi = 2\pi f$, is the radian frequency of the rf signal.

The effective dielectric constant, ε_{eff}, of the microstrip line can be affected by introducing a thin (thickness, t, $\leq$ about 1.5 μm) f-e film on top of the base

10   substrate used in Fig. 4b, and just beneath the metal layer. Bias can be applied to the line. Inductors of this type (single straight microstrip lines) are usually limited to L $\leq$ about 1.0 nH. Limiting factors are high resistance associated with a narrow W_L and current carrying

15   requirements as determined by the specific application. Similar inductive lines can be fabricated with bends or spirals, allowing for greater inductance, L, up to about 4.0 nH. Inductors of this type can also be fabricated as coplanar waveguide (CPW) or stripline topologies. Both the

20   inductance value, L, and the tuning range is limited in this approach. The use of thick film f-e fabrication may be

30

of greater benefit for tuning inductors, as it offers a potentially greater variation in ε_{eff} and Z_0.

An equivalent circuit model to the circuit in Fig. 4b is shown in Fig. 4c. The inductor 700 is shown as an
5 equivalent inductor 722 in Fig. 4c. There are also capacitors 724 and 726 which represent parasitic capacitances to ground of the microstrip portions 702 and 704 of Fig. 4b. Equivalent input and output planes A and A' are also shown in Fig. 4c. The input and output plane A is
10 coupled to the inductor 722 and to capacitor 724. Capacitor 724 is coupled to ground. Inductor 722 is also coupled to capacitor 726. Capacitor 726 is coupled to ground. Inductor 722 is also coupled to input and output plane A'.

The value of the shunt capacitors 724 and 726 can be
15 exploited in specific circuits. They can, for example, be absorbed by shunt capacitors situated adjacent to the inductor, on both sides.

The matching circuit may be of any topology that is known in the art. Several tunable matching circuits will
20 now be described. With reference to Fig. 5, a tunable matching circuit 122 is shown with a series tunable capacitor 125 and a shunt inductor 128 coupled between an input 131 and an output 134. Fig. 6 shows a tunable matching circuit 137 with a shunt inductor 140 and a series

31

capacitor 143 coupled between an input 146 and an output

149. Fig. 7 shows a tunable matching circuit 152 with a

series inductor 155 and a shunt capacitor 158 coupled

between an input 161 and an output 164. Fig. 8 shows a

5   tunable matching circuit 167 with a shunt capacitor 170 and

a series inductor 173 coupled between an input 176 and an

output 179. Alternatively, in any of Figs. 5-8, the

inductor 128, 140, 155, 173 may be tunable; or both the

capacitor 125, 143, 158, 170 and inductor 128, 140, 155,

10   173 may be tunable. Control voltages can be applied to the

f-e capacitor by means of the inductors shown in Figs. 5-8

in many cases. Alternatively, it may be applied to the f-e

capacitor by itself by proper design of the capacitor.

Figs. 9 and 10 show more complex matching circuits.

15   Fig. 9 is a block diagram of a pi matching circuit 102. The

pi matching circuit 102 has a first reactive element 106

coupled between an input 108 and ground 114. A second

reactive element 112 is coupled between the input 108 and

an output 116. A third reactive element 118 is coupled

20   between the output 116 and ground 114. Each reactive

element 106, 112, 114 may comprise either an inductor or a

capacitor. Any or all of the reactive elements may be

realized as lumped or distributed elemtns. At least one of

the reactive elements 106, 112, 114 is tunable. This allows

for the matching circuit 102 to be tunable.

Fig. 10 is a block diagram of a T matching circuit 60.

The T matching circuit 60 has a first reactive element 66

5   coupled between an input 63 and a second reactive element

69. The second reactive element 69 is coupled between the

first reactive element 66 and ground 72. A third reactive

element 75 is coupled between the first and second reactive

elements 66, 69 and an output 78. Each reactive element 66,

10   69, 75 may comprise either an inductor or a capacitor. Any

or all of the elements shown can be lumped or distributed

elements. At least one of the reactive elements 66, 69, 75

is tunable. This allows for the matching circuit 60 to be

tunable.

15   Figs. 5-10 show representative tunable matching

circuits. It will be understood that more complex matching

circuits may be constructed by combining the matching

circuits shown in Figs. 5-10 and by adding components in

series and in parallel with those components shown.

20   The capacitance of a f-e capacitor will always

decrease with increasing DC (control) voltage. The optimal

topology for a matching network must take this into

account. A Smith Chart is a useful tool for this purpose.

Historically, a Smith Chart was a graphical aid in which a

designer could plot the source or load impedance and then choose a matching circuit topology to move the source or load impedance to a desired location, typically to 50 Ω.

5   Alternatively, the f-e material's temperature dependence can be controlled by means of varying the DC control voltage as a function of temperature. One way this can be done is by means of a look-up-table stored in memory along with a temperature sensor, like a diode or thermistor.

10   F-E temperature dependence can be reduced by appropriate f-e material fabrication as well. In the preferred paraelectric state the material's Curie Temperature is below the operating temperature range. By moving the Curie point lower in temperature, one can

15 achieve less temperature variation in the f-e material. This comes at the expense of less tunability.

     The graphical Smith Chart has been implemented on many circuit simulation software packages in wide spread use. Examples are Eagleware(which has a separate matching

20 program as well) and Momentum. These tools can be used to choose the optimum or desirable matching circuit topology and the number of matching elements needed for a given application.

Fig. 11 is a block diagram showing a dielectric

tunable matching circuit 22 used to tune a device impedance

24 to a target impedance 26. The matching circuit 22 is

comprised of a capacitor 28 and an inductor 30. In a first

5   embodiment, the capacitor 28 may have a first dielectric

constant adjustment mechanism 34. Together, the capacitor

28 and the dielectric constant adjustment mechanism 34

comprise a tunable capacitor 32.

The dielectric constant adjustment mechanism 34

10 adjusts the dielectric constant of some or all of the

dielectric material proximate the capacitor 28. This shifts

the capacitance of the capacitor 28. This, in turn, shifts

the impedance of the device 51 and the matching circuit 22

combined. In this way, the impedance can be selectively

15 tuned to match the target impedance 26.

In a second embodiment, the inductor 30 may have a

second dielectric constant adjustment mechanism 33.

Together, the inductor 30 and the second dielectric

constant adjustment mechanism 33 comprise a tunable

20 inductor 31. The dielectric constant adjustment mechanism

33 adjusts the dielectric material proximate the inductor

30. This shifts the inductance of the inductor 30. This, in

turn, shifts the impedance of the device 51 and the

matching circuit 22 combined. In this way, the impedance can be selectively tuned to match the target impedance 26.

In a third embodiment, the matching circuit 22 may have both tunable components, that is, a tunable capacitor
5   32 and a tunable inductor 31.

In each of the first, second and third embodiments a first control source 96 or a second control source 98 or both will be present to send control signals to the dielectric constant adjustment mechanisms 34 and 33.

10   The matching of impedances is accomplished while maintaining very low total loss in the matching circuit 22. Five specific losses are shown in Fig. 11. There is a loss 53 associated with the first dielectric constant adjustment mechanism 34. This loss 53 may be the ferro-electric
15   material loss tangent, or L_{f-e}. There is a loss 55 associated with the capacitor 28. This loss 55 may be a combination of L_{metal} and L_{geom}. There is a loss 54 associated with the second dielectric constant adjustment mechanism 33. This loss 54 may be the ferro-electric material loss
20   tangent, or L_{f-e}. There is a loss 56 associated with the inductor 32. This loss 56 may be a combination of L_{metal} and L_{geom}. Finally, there is a loss 57 associated with the entire matching circuit 22. This loss 57 may be a combination of L_{attach}, L_{sub} and L_{rad}.

Each of these losses is eliminated or bounded by the techniques discussed above. Thus, this matching circuit 22 introduces sufficiently low loss to be usable in a wireless handset or other communication systems requiring low loss.

5   F-E tunable matching circuits can be used in several places in a wireless handset. Specifically, they can be used in, but are not limited to, matching an antenna to a duplexer, diplexer or multiplexer and for matching at the input and output of PA's and LNA's. They can also be used in the intermediate frequency (IF) strip to provide tuning there, if needed.

Fig. 12 shows a block diagram of two matching circuits 101 and 104 coupled to an amplifier 107. The amplifier 107 may be either a power amplifier (PA), a low noise amplifier (LNA) or any other suitable amplifier. The first matching circuit 101 sets the impedance seen by an input circuit 110 to a first target impedance. The target impedance may differ from the input impedance of the amplifier 107. The matching circuit 101 compensates for this difference. A second matching circuit 104 sets the impedance seen by the amplifier 107 to a second target impedance. The second target impedance may be equal to the first target impedance.

Matching can be achieved over a wider range of
frequencies while still maintaining the device's narrow
band characteristics. Being able to control the impedance
of an amplifier while it is being tuned reduces loss in the
5   signal path.

The control of matching circuits 101 and 104 may be
implemented by power sampling circuit 108, power detecting
circuit 103 and control circuit 105 as shown in Fig. 12.
Power sampling circuit 108 is coupled to the output of
10   amplifier 107. It samples the power output of amplifier 107
and transfers this signal to power detector circuit 103.
Power detect circuit 103 detects the power level of
amplifier 107 and transfers this signal to control circuit
105. Control circuit 105 receives the power level detected
15   by power detector circuit 103 as an input and produces a
control signal as an output. The control signal varies the
DC voltage applied to the f-e material in the matching
circuits 101 and 104. Thus, the matching circuits 101 and
104 are responsive to the power output of amplifier 107.

20   Together, power sampling circuit 108, power detecting
circuit 103 and control circuit 105 comprise a control
source. Note that power detector circuit 103 is shown as a
diode, a capacitor and an inductor for the purpose of
illustration only. Any suitable power detector may be used.

38

An alternate control source is shown in Fig. 15. A
band select signal is received as an input 237 to control
source 221. Control source 221 comprises a voltage source
223 and a look-up table 229. Responsive to the band select

5   signal, the control source 221 looks up a value in the
look-up table 229 corresponding to the band selected. The
value represents a voltage to be applied by the control
source 221 to the matching ciruit 225. The voltage
comprises a control signal, changing the impedance of the

10 matching circuit 225.

F-E tuning in PA's can not only electrically adjust
the output impedance match for a given device initially and
optimize it over temperature, but can also dynamically vary
the load line of a PA given the known required power

15 output. The ability to optimize a PA's load line under a
wide range of output power is key to obtaining optimum
power efficiency and thus minimizing the power consumption
on the D.C. power source, i.e., a battery in the case of
wireless handsets. This increases talk time and reduces

20 heat dissipation.

The maximum output power that a f-e tunable amplifier
can handle is limited by the f-e material's non-linearity
and the overall system requirements. For wireless handsets
there are appropriate standards, like IS-95 or IS-98, that

define the tolerable limits on transmit (PA) non-linearity in terms of adjacent and/or co-channel interference. Improving a PA's linearity has a direct, positive effect in that a smaller device and/or less bias current needs to be

5   used to meet these standards. The linearity of the f-e material must be considered. The f-e materials described herein have some non-linearity. The particular choice of f-e film will be determined by the tolerance of a given system to non-linearity.

10   Additionally, increased output power can be achieved by conventional paralleling of devices, as is apparent to anyone skilled in the art. F-E tunability can be exploited in these cases as well.

F-E materials can also benefit LNA's. LNA's can

15   electrically adjust for the optimum input impedance match of a device, along with the output, to provide for optimum noise figure and intercept point. As is the case of the PA, this can be controlled over temperature, as well. Amplifier performance changes over temperature. This may create

20   impedance mismatches at different temperatures and/or a shift in the active device's operating point. F-E tunability can be used to compensate for this impedance mismatch by appropriate choice of:

1) f-e material temperature characeristics, and/or;

2) matching topology chosen.

Tunability allows for an LNA and a PA to be operated optimally over more than one band. This is especially useful in wireless handsets because the amount of space in
5 a handset is limited and many operating bands are closely spaced. Space savings are proportional to the number of independent components for different bands that are eliminated by adding tunable components. Tunability allows a handset manufacturer to have fewer different PA and LNA
10 designs on hand to build handsets for a diverse market. It also allows for operation of handsets over wide geographic regions without requiring multiple PA's and LNA's. For example, one PA or LNA can cover multiple PCS bands, such as, for example, the Korean, Indian, and U.S. PCS bands.
15 The resulting improved match will translate to increased antenna gain, further improving handset performance, both for the transmit side (lower required PA power, more linearity) and the receive side (increased sensitivity, less LNA bias current needed).

20 Another example of a tunable matching circuit is a matching circuit for matching an impedance of an antenna to the impedance of either a duplexer or a diplexer. These configurations are shown in Figs. 13 and 14. In Fig. 13, an antenna 42 is coupled to a matching circuit 44. The

matching circuit 44 is coupled to a duplexer 46. The

matching circuit 44 sets the impedance seen by the antenna

42 to a target impedance. The target impedance may be

different from the input impedance of the duplexer 46. The

5   matching circuit 44 compensates for this difference. The

matching impedance also sets the impedance seen by the

duplexer 46 to a target impedance. This target impedance

may be different from the input impedance of the antenna

42. The matching circuit 44 compensates for this

10   difference.

In Fig. 14, an antenna 48 is coupled to a matching

circuit 50. The matching circuit 50 is coupled to a

diplexer 52. The matching circuit 50 sets the impedance

seen by the antenna 48 to a target impedance. The target

15   impedance may be different from the input impedance of the

diplexer 52. The matching circuit 50 compensates for this

difference. The matching impedance also sets the impedance

seen by the diplexer 52 to a target impedance. This target

impedance may be different from the input impedance of the

20   antenna 48. The matching circuit 50 compensates for this

difference. The diplexer is shown as providing for the PCS

and cellular bands. This is by way of example only. The

diplexer could provide for other bands, it could be

replaced by a multiplexer providing for more than two bands.

Note that a control signal is applied to the matching ciruits 44 and 50 of Figs. 13 and 14, respectively. This control signal may be generated in a manner similar to those in Figs. 12 or 15, or any other suitable method. A power sampler may be applied, for example at the duplexer 46 Tx or Rx ports, or at the diplexer PCS or cellular ports.

The resulting improved match will translate to increased antenna gain, further improving handset performance, both for the transmit side (lower required PA power, more linearity) and the receive side (increased sensitivity, less LNA bias current needed).

Although the invention has been described with reference to particular embodiments, the description is only an example of the invention's application and should not be taken as a limitation. Consequently, various adaptations and combinations of features of the embodiments disclosed are within the scope of the invention as encompassed by the following claims.